REMARKS

I. Status of the Application

Claims 15-28 are pending in this application. In the January 26, 2005 office action, the Examiner:

A. Rejected claims 18, 23 and 24 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the written description requirement;

B. Rejected claims 18, 23 and 24 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite;

C. Rejected claims 15-17, 22, 25, 26 and 28 under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 6,208,183 to Li et al. (hereinafter "Li");

D. Rejected claims 19-21 under 35 U.S.C. § 103(a) as allegedly being obvious over Li in view of one of U.S. Patent No. 6,373,913 to Lee et al. (hereinafter "Lee") or U.S. Patent No. 6,469,559 to Heightley (hereinafter "Heightley); and

E. Deemed claim 27 allowable if rewritten in independent form.

In this response, applicants have amended claims 15 and 22, and have canceled claims 17, 18, 23, 24 and 27, without prejudice. Applicants have further added new claims 29-38. Applicants respectfully traverse the rejection of claims and request reconsideration in view of the foregoing amendments and the following remarks.

II. The 35 U.S.C. § 112 Rejections Are Moot

The Examiner has rejected claims 18, 23 and 24 under the first and second paragraphs of 35 U.S.C. § 112. Applicants traverse the rejection. However, for convenience, those claims have been canceled. Accordingly, it is respectfully submitted that the 35 U.S.C. § 112 rejections of claims 18, 23 and 24 are moot.

III. Claim 15 is Patentable Over the Prior Art

In the January 26, 2005 office action, the Examiner rejected claim 15 as being allegedly being anticipated by Li. For reasons discussed below in detail, it is respectfully submitted that claim 15 is allowable over Li.

A. The Present Invention

Claim 15 is directed to a delay lock loop apparatus for use with an externally generated clock signal. The apparatus includes a delay device, a feedback device, a frequency detection device and a phase difference detection device.

The delay device includes a first delay element and a second delay element. The first delay element is configured to generate a first output responsive to a control signal and a first input, and the second delay element is configured to generate the first input responsive to the externally generated clock signal and a set signal related to the frequency of the externally generated clock signal. The feedback device is operably connected to the first delay element and configured to generate a time delayed first output. As amended, the feedback device is

operable to delay the first output by an amount substantially equal to a receiver time delay plus a driver time delay. The added limitation is similar to the limitation of claim 17.

The phase difference detection device is configured to generate signal responsive to the phase difference between the time delayed first output and the externally generated clock signal. The frequency detection unit is configured to generate the set signal responsive to the frequency of the externally generated clock signal.

B. Li Does Not Teach a Feedback Element that Introduces a Delay Substantially Equal to a Receiver Time Delay and a Driver Time Delay

Li shows a gated-delay locked loop that generates an output clock signal that is in phase with, and has a frequency which is an integer multiple of, a reference clock. Contrary to the present invention, Li fails to teach or fairly suggest a feedback device that is operable to delay the first output by an amount substantially equal to a receiver time delay plus a driver time delay, as called for in claim 15.

In general, the Examiner correctly noted that some delay is necessarily created by the feedback frequency divider 308 of Li. In support of this, the Examiner cited the teaching of column 11 of Li, which states, "Maintaining Θ_{fix} at a constant value can be problematic since the *delay* contributed by frequency divider 308 may vary". (Li at col. 11, lines 48-50) (emphasis added). Upon reading in further context, however, Li only teach suggests that the frequency divider 308 produces an indiscriminate delay, presumably unintentionally created. There is no indication that this delay is substantially equal to any receiver time delay or driver time delay.

Furthermore, there appears to be a need to compensate for the variability of the delay created by the frequency divider. Specifically, the sentences following the above quoted sentence reads "To resolve this problem, GDLL 300 utilizes a voltage-controlled delay 314 rather than a fixed delay. Voltage-controlled delay 314 is adjusted as necessary by a second delay-locked loop 330 to maintain a constant Θ_{fix}." (*Id.* at col. 11, lines 50-53). Thus, if the delay of the frequency divider 308 is referenced as a "problem", it does not suggest that the delay introduced thereby is affirmatively configured to be equal to any delays associated with a receiver or driver circuit.

Accordingly, Li does not teach or suggest that the frequency divider 308 has a delay configured to be (or accidentally being) substantially equal to the driver time delay and the receiver time delay.

As discussed further above, the limitation added by the amendment to claim 15 is substantially identical to the limitation recited in claim 17 as originally filed. The Examiner rejected claim 17, stating that col. 6 of Li taught the claimed delay. (Office action at p.4). In particular, the Examiner stated that "col. 6, lines 55-65, discloses the output of the feedback device being determined by a receiver time delay (phase delay) and a driver time delay (Kdel)." The cited portions of Li are set forth below:

> The Laplace transform of the transfer function of DLL 100 can be expressed as:
>
> $$\Theta_{out} - \Theta_{in} = \Theta_{del}(V)$$
>
> where Θ_{out} is the phase of the output signal of the VCD, Θ_{in} is the phase of the input signal to the VCD, and V is the voltage applied to the controlled input of the VCD. Assuming that $\Theta_{del}(V)=K_{del}V$, where K_{del} is the gain of VCD 110; and $V=K_{\Theta}(\Theta_{out} - \Theta_{in}-2\pi N)Z(s)$, where K_{Θ} is the gain of the phase detector 102, Z(s) is the transfer function of the loop filter 106, and N is a positive integer representing the division factor implemented through the frequency divider 108, . . .

(Li at col. 6, lines 53-65).

It is respectfully submitted that the above quoted paragraph does not describe *any* delay added by the frequency divider 108. Accordingly, such a paragraph cannot support the implication that *any* frequency divider, either 108 or 308 provides *any* delay, much less the claimed delay amount.

Accordingly, for this additional reason, it is respectfully submitted that Li does not teach a feedback device that generates a delay substantially equal to a receiver time delay and a driver time delay.

Finally, elsewhere in the office action, the Examiner appears to allege that this limitation is the limitation that causes claim 27 to have patentable subject matter. In particular, the Examiner stated that "none of the prior art teaches or fairly suggests, among other things, the limitation '*time delaying the further delayed external clock signal by an amount of time equal to the receiver time delay plus the driver time delay*'". (Office Action at p.6). While the Examiner *may* have been referring to this limitation *exclusively* within the context of claims 22 and 27, it can nevertheless be reasonably concluded that this limitation creates a patentable distinction to the general subject matter of *both* claims 15 and 22.

For any and all of the foregoing reasons, it is respectfully submitted that claim 15 is patentable over the prior art. Accordingly, the rejection of claim 15 should be withdrawn.

IV. Claims 16 and 19-21

Claims 16 and 19-21 all stand rejected as allegedly being anticipated by, or obvious over, Li. Claims 16 and 19-21 depend from and incorporate all of the limitations of claim 15. Neither of the secondary references is cited as teaching a feedback device that creates a delay substantially equal to a receiver time delay and a driver time delay. Accordingly, for at least

the same reasons as those set forth above in connection with claim 15, it is respectfully that the rejection of claims 16 and 19-21 should be withdrawn.

V. Claim 22

Claim 22 has been amended to incorporate the limitation recited above in connection with claim 15, except that the "feedback device" is not positively recited. As also discussed above, the Examiner alleged that claim 27 would be allowable if rewritten in independent form. The amendments to claim 22 incorporate the salient allowable subject matter of claim 27.

In particular, the Examiner stated that "none of the prior art teaches or fairly suggests, among other things, the limitation '*time delaying the further delayed external clock signal by an amount of time equal to the receiver time delay plus the driver time delay*'" . (Office Action at p.6). Claim 22, as amended, recites "*further delaying the delayed external clock signal with the first variable delay element by an amount of time equal to the received time delay plus the driver time delay*". Thus, claim 22 now includes the subject matter deemed patentable by the Examiner.

Accordingly, it is respectfully submitted that the rejection of claim 22 should be withdrawn.

V. Claims 25, 26 and 28

Claims 25, 26 and 28 all stand rejected as allegedly being anticipated by, or obvious over, Li. Claims 25, 26 and 28 depend from and incorporate all of the limitations of claim 22. Neither of the secondary references is cited as further delaying a signal by an amount

substantially equal to a receiver time delay and a driver time delay. Accordingly, for at least the same reasons as those set forth above in connection with claim 22, it is respectfully that the rejection of claims 25, 26 and 28 should be withdrawn.

VI. New Claims 29-38

New claim 29 is similar to claim 15 as originally filed. However, new claim 29 includes a limitation directed to "a frequency detection unit coupled to *directly* receive the externally generated clock signal". Li fails to teach such a limitation. Li instead teaches that the frequency detection unit 332 is coupled to the *output* of the second delay element, the VCD 314. The output of the VCD 314 is *not* the externally generated clock signal. Accordingly, a connection to the output of the VCD 314 is not a connection that directly receives the externally generated clock signal.

As a consequence, Li fails to teach a frequency detection unit, connected as claimed, and which is coupled to *directly* receive the externally generated clock signal. For at least this reason it is respectfully submitted that claim 29 is allowable over the prior art.

Claims 30-38 all depend from and incorporate all of the limitations of claim 29. Accordingly, claims 30-38 are allowable over the prior art for at least the same reasons.

VII. Conclusion

For all of the foregoing reasons, it is respectfully submitted the applicants have made a patentable contribution to the art. Favorable reconsideration and allowance of this application is, therefore, respectfully requested.

Respectfully submitted,

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